David H. K. Hoe

Loyola University Maryland
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Research Interests

Analog and mixed-signal integrated circuit design, bio-inspired circuits and signal processing, high-performance computing, field programmable gate array (FPGA) design

Academic Appointments

Loyola University Maryland, Baltimore, MD
Assistant Professor, Dept. of Engineering, 2014 – present
Courses taught: Introduction to Microprocessor-based Systems, Electronics, Signals and Systems, Linear Circuits Analysis, Digital Logic, FPGA Design

University of Texas at Tyler, Tyler, TX
Assistant Professor, Dept. of Electrical Engineering, 2008 – 2014
Courses taught: VLSI Design, FPGA Design, RF CMOS IC Design, Computer Architecture, Digital Signal Processing, Signals and Systems, Linear Circuits II

University of Texas at Arlington, Arlington, TX
Adjunct Professor/Research Associate, Dept. of Electrical Engineering, 1997 – 2002, 2008
Courses taught: VLSI Design, Analog CMOS IC Design, Advanced Analog VLSI Systems

Dallas Theological Seminary, Dallas, TX
Adjunct Professor, New Testament Dept., 2001 – 2008
Courses taught: Introductory Greek Grammar, Intermediate Greek Grammar

Industry Experience

General Electric Corporate Research and Development Center, Schenectady, NY
Staff Engineer, 1991 – 1996
Design of analog integrated circuits for medical systems applications

Education

University of Toronto, Toronto, Canada
Ph.D., Electrical Engineering, 1991
Thesis: *High-Speed GaAs Dynamic Logic*, Advisor. Dr. C. A. T. Salama

M.A.Sc., Electrical Engineering, 1988
Thesis: *A CMOS Compatible Single Poly EPROM*, Advisor, Dr. C. A. T. Salama

B.A.Sc., Engineering Science, 1987 (Hons.)

Dallas Theological Seminary, Dallas, TX
Th.M., Academic Ministries, 1999

Publications (*Peer Reviewed*)

(* indicates undergraduate student co-author)

Journal Papers

D. H. K. Hoe, "Mitigating Autocorrelation in Stochastic Logic: A Study of Simplified Buffering Schemes for Bayesian Inference," *VLSI Design* (under review)

D. H. K. Hoe and X. Jin, "The Design of Low Noise Amplifiers in Deep Submicron CMOS Processes: A Convex Optimization Approach," *VLSI Design*, September 2015.

D. H. K. Hoe, L. P. D. Bollepalli, and C. D. Martinez*, "FPGA Fault Tolerant Arithmetic Logic: A Case Study Using Parallel-Prefix Adders," *VLSI Design*, Nov. 2013.

D. H. K. Hoe, J. M. Comer*, J. C. Cerda*, C. D. Martinez*, M. V. Shirvaikar, "Cellular Automata-based Parallel Random Number Generators using FPGAs," *International Journal of Reconfigurable Computing*, June 2012.

D. H. K. Hoe and D. B. Ribner, "An Auto-ranging Photodiode Preamplifier with 114dB Dynamic Range," *IEEE. J. Solid-State Circuits*, pp. 187-194, Feb. 1996.

D. H. K. Hoe and C. A. T. Salama, "GaAs Trickle Transistor Dynamic Logic," *IEEE. J. Solid-State Circuits*, vol. SC-26, pp. 1441-1448, Oct. 1991.

D. H. K. Hoe and C. A. T. Salama, "Dynamic GaAs Logic Circuits," *International. J. High Speed Electronics*, vol. 2, pp. 163-183, Sept. 1991.

D. H. K. Hoe and C. A. T. Salama, "Dynamic GaAs Capacitively Coupled Domino Logic," *IEEE. J. Solid-State Circuits*, vol. SC-26, pp. 844-849, June 1991.

S. Liang, D. H. K. Hoe, C.A.T. Salama, "BiCMOS DCVSL gate," *Electronics Letters*, vol. 27, no. 4, pp. 346-347, 14 Feb. 1991.

D. H. K. Hoe, C.A.T. Salama, "GaAs capacitively coupled domino logic gate," *Electronics Letters*, vol. 25, no. 25, pp. 1714-1715, 7 Dec. 1989.

D. H. K. Hoe, K. J. Schultz, C. A. T. Salama, R. A. Hadaway and P. Kempf, "Cell and Circuit Design for Single-Poly EPROM," *IEEE J. Solid-State Circuits*, vol. SC-24, pp. 1153-1157, Aug. 1989.

K. J. Schultz, D. H. K. Hoe and C.A.T. Salama, "A microprogrammable processor using single poly EPROM," *Integration*, vol. 8, pp. 189-199, Aug. 1989.

<u>Conference Proceedings</u> (Research – *Peer Reviewed*)

D. H. K. Hoe, "Bayesian Inference using Spintronic Technology: A Proposal for an MRAM-based Stochastic Logic Gate," *Proceedings of IEEE 60th International Midwest Symposium on Circuits and Systems*, pp. 1521-1525, August 2017.

H. A. Ochoa, D. H. Hoe, D. Veeramachaneni, "The Implementation of Compressive Sensing on a FPGA for Chaotic Radars," *SPIE DSS Conference*, April 2015.

D. H. K. Hoe, J. Rajendran, R. Karri, "Towards Secure Analog Designs: A Secure Sense Amplifier Using Memristors," *IEEE Computer Society Annual Symposium on VLSI*, July 2014.

J. F. Johnson* and D. H. K. Hoe, "Designing an Agent Based Model for the Efficient Removal of Red Imported Fire Ant Colonies," *SummerSim Conference 2013*, July 2013.

I. Olmedo*, Y. Guerra Perez*, J. F. Johnson*, L. Raut*, and D. H. K. Hoe, "Image Segmentation on GPGPUs: A Cellular Automata-based Approach," *SummerSim Conference 2013*, July 2013.

L. Raut* and D. H. K. Hoe, "Stream Cipher Design Using Cellular Automata Implemented on FPGAs," *IEEE 45th Southeastern Symposium on System Theory*, March 2013.

D. H. K. Hoe, "The Use of Error Correcting Codes for Nanoelectronic Systems: Overview and Future Prospects," *IEEE 45th Southeastern Symposium on System Theory*, March 2013.

X. Jin and D. H. K. Hoe, "Optimization of Short Channel CMOS LNAs by Geometric Programming," *IEEE 55th International Midwest Symposium on Circuits and Systems*, pp. 9-12, August 2012.

J. C. Cerda*, C. D. Martinez*, J. M. Comer*, and D. H. K. Hoe, "An Efficient FPGA Random Number Generator using LFSRs and Cellular Automata," *IEEE 55th International Midwest Symposium on Circuits and Systems*, pp. 912-915, August 2012.

J. M. Comer*, J. C. Cerda*, C. D. Martinez*, D. H. K. Hoe, "Random Number Generators Using Cellular Automata Implemented on FPGAs," *IEEE 44th Southeastern Symposium on System Theory*, pp. 67-72, March 2012.

R. J. Gera and D. H. K. Hoe, "An Evaluation of CMOS Adders in Deep Submicron Processes," *IEEE 44th Southeastern Symposium on System Theory*, pp. 126-129, March 2012.

C. D. Martinez*, L. P. D. Bollepalli, D. H. K. Hoe, "A Fault Tolerant Parallel-Prefix Adder for VLSI and FPGA Design," *IEEE 44th Southeastern Symposium on System Theory*, pp. 121-125, March 2012.

D. H. K. Hoe, C. Martinez*, and J. Vundavalli, "Design and Characterization of Parallel Prefix Adders using FPGAs," *IEEE 43rd Southeastern Symposium on System Theory*, pp. 170-174, March 2011.

D. H. K. Hoe, "Fault Tolerant Cellular Array Design for Nanoscale Technologies," *IEEE 42st Southeastern Symposium on System Theory*, pp. 258-262, March 2010.

S. K. Haridass and D. H. K. Hoe, "Fault Tolerant Block Based Neural Networks," *IEEE 42st Southeastern Symposium on System Theory*, pp. 357-361, March 2010.

D. H. K. Hoe, "A Reconfigurable Dynamic Logic Cell for Programmable Datapaths," IEEE 41st Southeastern Symposium on System Theory, March 2009.

Conference Proceedings (Education – *Peer Reviewed*)

D. H. K. Hoe, "Promoting Undergraduate Research in the Electrical Engineering Curriculum," *ASEE 2014 Annual Conference & Exposition*, June 2014.

D. H. K. Hoe, "Development of a Concept Inventory for Microelectronics Classes," *Frontiers in Education Conference (FIE),* October 2013.

D. H. K. Hoe, "Introducing Nanoelectronics into the Electrical Engineering Curriculum," *ASEE 2013 Annual Conference & Exposition*, June 2013.

D. H. K. Hoe, "The Impact of Peer Interaction Exercises in a Signals and Systems Course," *ASEE Gulf Southwest Annual Conference*, March 2013 (*2013 ASEE Zone 3 Best Paper award*).

D. H. K. Hoe, "Undergraduate Research Experiences using FPGAs," *ASEE 2012 Annual Conference & Exposition*, June 2012.

D. H. K. Hoe, "Introducing Multiple Soft Processor Cores Using FPGAs into the Computer Engineering Curriculum," *ASEE 2012 Annual Conference & Exposition*, June 2012.

D. H. K. Hoe, "Integration of a Structured Inquiry-based Approach into Microelectronic Classes," *ASEE Gulf Southwest Annual Conference*, April 2012.

D. H. K. Hoe and M. Shirvaikar, "Introduction of Semiconductor Test Engineering into the BSEE Curriculum," *ASEE 2011 Annual Conference & Exposition*, June 26-29, 2011.

Invited Presentations

D. H. K. Hoe, "Cellular Automata, Field Programmable Gate Arrays, Undergraduate Research" *University of Texas at Arlington,* Arlington, TX, April 24, 2015.

M. R. Rudra, N. A. Daniels, N. Varum, D. H. K. Hoe, "Designing Stealthy Trojans with Sequential Logic: A Stream Cipher Case Study," *IEEE/ACM Design Automation Conference (DAC)*: *Special Session on the Embedded Systems Challenge 2013*, June 2014.

Awards to Students

John Harten, "Hybrid Cellular Automata with Nonlinear Feedback Shift Registers," second place in the Natural & Applied Sciences Poster Session, Undergraduate Student Research & Scholarship Colloquium, on April 9, 2016 at Loyola University Maryland. Advisor: D. Hoe

M. R. Rudra, N. Daniels, N. Varum, "Effective Trojan Implementation on Stream-Cipher based Encryption Circuit," third place at the *Embedded System Challenge 2013*, Nov 16, 2013 at NYU-Poly, Brooklyn, NY. Advisor: D. Hoe

Irving Olmedo, James Johnson and Yessika Guerra Perez, "Image Segmentation Algorithm for General Purpose Graphical Processing Units," third place at the IEEE R5 Regional paper competition in Denver, CO on April 6, 2013. Advisor: D. Hoe

Lakshman Raut, "Stream Cipher Design Using Cellular Automata Implemented on FPGAs," first place in the engineering category at the NSF LSAMP State-wide poster competition, El Paso, TX, September 21, 2012. Advisor: D. Hoe

Service

Curriculum Revision Committee, Engineering Department, Member, Spring 2015 - present

Loyola Robotics Club, Faculty Advisor, Spring 2015 – present

Bible Study for faculty and students in the Engineering Department, Leader, Spring 2015 – present

National Fellowships Committee, Member, Fall 2015 – Spring 2016

Professional Memberships

Institute of Electrical and Electronic Engineers

Council for Undergraduate Research

Cosmos and Creation